

## REMARKS

All of the claims were rejected over a couple of pages out of a computer architecture book. The material cited is so vague and incomplete that there is no basis whatsoever to conclude that the so-called functional units constitute separate processors. Therefore, a *prima facie* rejection is not made out, since there is no showing that a register is accessible by a plurality of processors.

There is no reason to believe that the functional units are separate processors. Moreover, there is no indicating whether data in said register is available for a given processor. To show this element, five pages are cited in Figure 4.4. But Figure 4.4 shows nothing of the sort and the five pages have nothing informative.

Therefore, reconsideration of the rejection of claim 1 and its dependent claims is respectfully requested. On the same basis, claim 11 and its dependent claims is respectfully requested.

Claim 18 calls for a plurality of processing elements. But there is no indication that the functional units integer, MULT1, etc. constitute processing elements. Moreover, there is no structure shown and, therefore, it cannot be determined that a register is coupled to said processing elements. Moreover, there is no indication in the material cited that the register includes a plurality of general purpose registers. There is no basis for concluding that one of the registers indicates whether the data in the register is available for a given one of said plurality of processing elements.

Therefore, reconsideration of rejection of claim 18 and its dependent claims is respectfully requested.

In view of these remarks, the application should now be in condition for allowance.

Respectfully submitted,

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